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심사청구 : 있음

(54) 피-채널 이중확산 전력소자의 제조방법

요약

본 발명은 필드 산화막으로서 TEOS 산화막을 형성한 MOS형 P-채널 이중확산 고 전압 전력소자의 제조방법을 제공한다.

본 발명에 따르면, 종래의 고전압 전력소자의 제조에 있어서 문제시되는 필드 산화막의 새부리(Bird's beak)에 의한 드리프트 영역의 확대를 방지하기 위해, 저온에서 형성이 가능한 TEOS 산화막을 형성하고, 이 TEOS 산화막을 경사식각하여 길이가 짧은 필드 산화막을 형성하여 드리프트 영역의 길이를 감소시켰다.

따라서, 본 발명은 열산화법에 의해 필드산화막을 형성하는 종래의 기술에 비하여 드리프트 영역의 길이를 감소시키는 동시에, 드리프트 영역에 주입된 불순물의 외부확산이 방지되어 전력소자의 ON-저항이 개선된다.

명세서

도면의 간단한 설명

도 1은 종래의 이중 확산된 P-채널 고전압 전력소자의 단면도,

도 2a는 본 발명에 의한 P-채널 고전압 전력소자의 단면도,

도 3a 내지 도 3g는 본 발명에 의한 P-채널 고전압 전력소자의 제조 공정을 순서대로 나타낸 공정 단면도,

도 4는 필드 산화막 형성 후 드리프트 영역에서의 불순물 농도를 나타낸 단면도,

도 5는 LOCUS 기술을 이용하여 필드 산화막을 형성한 전력소자와 TEOS 식각기술을 이용하여 필드 산화막을 형성한 전력소자의 전류-전압 특성을 나타낸 그래프.

<도면의 주요 부분에 대한 부호의 설명>

20 : 기판 1,21 : 매몰 산화층층
3,22 : P-에피층 3,23 : 깊은 N-웰
4,24 : P-드리프트 영역 5,25 : N-웰
6,26 : 필드 산화막 7,27 : 게이트 산화막

PATENT ABSTRACTS OF JAPAN

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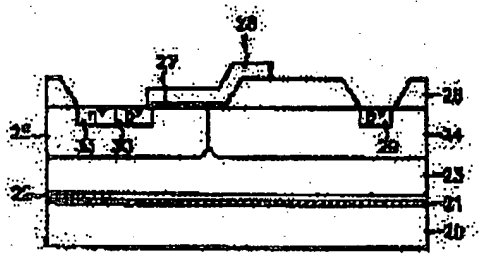
(30)Priority
Priority number : 97 9761585 Priority date : 20.11.1997 Priority country : KR

(54) FABRICATION OF HIGH VOLTAGE POWER ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To improve on-resistance by minimizing impurity diffusion of drift region and decreasing the length thereof using a TEOS oxide which is deposited through low temperature field oxide deposition process in the fabrication process of MOS high voltage power element.
SOLUTION: A P-epitaxial layer 22 is implanted with phosphorous ions and heated treated to form a deep N-well 23, and an ion implanted mask defining a float region is formed thereon. Subsequently, P-type impurity ions are implanted and an ion-implanted mask defining an N-well is formed on the deep N-well 23 and then is heated-treated to form a P-type drift region 24 an N-well 25 abutting thereon. Thereafter, an oxide is deposited on the entire surface of the substrate, a primary TEOS oxide is deposited and heat treated, a thinner secondary TEOS oxide is further deposited thereon and etched to form a field oxide 26, in which a specified region is exposed in the active region of a power element.



LEGAL STATUS

[Date of request for examination] 13.10.1998

[Date of sending the examiner's decision f rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registrati n]

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CLAIMS

[Claim(s)]
[Claim 1] A manufacture method of a high-tension power element characterized by providing the following The 1st step which forms the 1st well of the 1st conductivity type in an epitaxial layer of the semiconductor substrate upper part The 2nd step which forms a drift region of the 2nd conductivity type, and the 2nd well of the 1st conductivity type in the 1st well of the above The 3rd step which forms a TEOS oxide film in the whole structure upper part after the 2nd-step above-mentioned execution The 4th step which forms field oxide which carries out the selection chemical engraving of the above-mentioned TEOS oxide film, and defines an active region, the 5th step which forms the above-mentioned gate insulator layer and a gate electrode, and the 6th step which forms the source / drain field of the 2nd conductivity type in the above-mentioned active region
[Claim 2] A manufacture method of a high-tension power element according to claim 1 characterized by including further the 7th step which forms a pad oxide film of 200 thru/or 500A thickness in the whole structure upper part after the 2nd-step above-mentioned execution.
[Claim 3] The 3rd above-mentioned step is the manufacture method of a high-tension power lement according to claim 2 characterized by coming to contain the 8th step which vapor-deposits the 1st TEOS oxide film of 5000 thru/or 8000A thickness on the above-mentioned pad oxide film, the 9th step which heat-treats the above-mentioned 1st TEOS oxide film, and the 10th step which forms the 2nd TEOS oxide film of 2000 thru/or 3000A thickness on the above-mentioned 1st TEOS oxide film.
[Claim 4] The above-mentioned selection chemical engraving in the 4th above-mentioned step is the manufacture method of a high-tension power element according to claim 1 characterized by using the dip etching method which used diluted HF solution.
[Claim 5] A manufacture method of a high-tension power element according to claim 1 to 4 characterized by for the 1st conductivity type of the above being N type, and the 2nd conductivity type of the above being P type.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the manufacture method of an MOS mold high-tension power element about semiconductor technology.
[0002]
[Description of the Prior Art] Generally, the P type high-tension power element for 100 - 500V is manufactured using the MOS technology of a water Heiji pile diffusion mold, and is used for the actuation IC (integratedcircuit) of a step motor (step motor), and FED (field emission display) and PDP (plasma display panel) etc.
[0003] In order to improve the breakdown voltage and ON-resistance of a power element using N-drift (drift) field formed by the high N type epitaxial layer of specific resistance on the P type (or N type) semiconductor substrate in the former in order to embody a water flat tip power element with high breakdown voltage, many technology of attaining structural change of an lement and improving a process has been developed.
[0004] Such a conventional method has improved breakdown voltage by determining a vertical and horizontal breakdown voltage value, forming a metal electrode (metal electrode) in the metal electric-field version (field plate) or a drain field for a long time, and making the strength of electric field ease with epitaxial layer thickness and high impurity concentration, the thickness of a drift region, and the concentration of an impurity.
[0005] Although many improvements were made in the breakdown voltage and ON-resistance of P-mold power element until now, it must be improved further, and since ON-resistance will come to increase according to it if breakdown voltage is lowered, development of the technology for optimization of two kinds of these elements is demanded.
[0006] Drawing 10 will be a thing illustrating the cross-section structure of the water flat tip P-channel high-tension power element formed by the conventional technology, and hereafter, if the manufacturing process is roughly considered with reference to this, it will be as follows. First, the embedded oxide layer 1, the P type epitaxial layer 2, and the deep N-well 3 are formed in order on the semiconductor substrate 20, and the P type drift region 4 and the N-well 5 are formed on the deep N-well 3. The field oxide 6 which defines the active region and the non-active region of an element as the degree using LOCOS (local oxidation of silicon) technology is formed, and gate oxide 7 and the polycrystal silicon gate 8 are formed on the substrate of the field where the P type drift region 4 and the N-well 5 touch.
[0007] Continuously, a P type impurity ion implantation is carried out to the predetermined field of the P type drift region 4 and the N-well 5, and the source field 10 and the drain field 9 are formed in it. Subsequently, after forming N+ mold source contact 13 which carries out an N type impurity i n implantation and touches the source field 10, manufactur of an element is completed by f rming the interlay r insulation film 11 to which som f the source field 10 and drain fields 9, N+ mold source contacts 13, and gate electrodes 8 are exposed, applying a metal to the whole surface, carrying out patterning of this by the photolithography meth d, and forming a metal electrode 12.

[0008]
[Problem(s) to be Solved by the Invention] However, the above is in process, and in order to form field oxide 6, the thermal oxidation process of the long duration which advances at a 1000-d gree C elevated temperature is needed. To that external diffusion of the impurity pour d int th drift region 4 while the field oxid 6 formation process advanced in connecti n with this occurs, and coincidence Oxide-film growth to the side and the perpendicular direction by the BAZU beak (bird'sbeak) effect of field oxide in a lateral portion occurs. Since it is expanded from a layout value as the length of the formation field of field oxide 6 is shown by A from the length (layout value) of the mask pattern for forming field oxide 6, the trouble which ON-resistance comes to increase is induced.
[0009] This invention was made in order to cancel the trouble concerning the conventional example mentioned above, and it tends to offer the manufacture method of a high-tension power element that impurity external diffusion of a drift region is minimized, the length of a drift region is reduced, and ON-resistance can be improved.
[0010]
[Means for Solving the Problem] The 1st step where a manufacture method of a high-tension power element concerning this invention forms the 1st well of the 1st conductivity type in an epitaxial layer of the semiconductor substrate upper part, The 2nd step which forms a drift region of the 2nd conductivity type, and the 2nd well of the 1st conductivity type in the 1st well of the above, The 3rd step which forms a TEOS oxide film in the whole structure upper part after the 2nd step execution of an account, The 4th step which forms field oxide which carries out the selection chemical engraving of the above-mentioned TEOS oxide film, and defines an active region, the 5th step which forms the above-mentioned gate insulator layer and a gate electrode, and the 6th step which forms the source / drain field of the 2nd conductivity type in the above-mentioned active region are included.
[0011] Moreover, it is characterized by including further the 7th step which forms a pad oxide film of 200 thru/or 500A thickness in the whole structure upper part after the 2nd-step above-mentioned execution.
[0012] Moreover, it is characterized by the 3rd above-mentioned step coming to contain the 8th step which vapor-deposits the 1st TEOS oxide film of 5000 thru/or 8000A thickness on the above-mentioned pad oxide film, the 9th step which heat-treats the above-mentioned 1st TEOS oxide film, and the 10th step which forms the 2nd TEOS oxide film of 2000 thru/or 3000A thickness on the above-mentioned 1st TEOS oxide film.
[0013] Moreover, the above-mentioned selection chemical engraving in the 4th above-mentioned step is characterized by using the dip etching method which used diluted HF solution.
[0014] Furthermore, it is characterized by for the 1st conductivity type of the above being N type, and the 2nd conductivity type of the above being P type.
[0015]
[Embodiment of the Invention] The 1st step where the high-tension power element manufacture method concerning this invention forms the 1st well of the 1st conductivity type in the epitaxial layer of the semiconductor substrate upper part, The 2nd step which forms the drift region of the 2nd conductivity type, and the 2nd well of the 1st conductivity type in the 1st well of the above, The 3rd step which forms a TEOS oxide film in the whole structure upper part after the 2nd-step above-mentioned execution,

* NOTICES *

TECHNICAL FIELD

[A technical field to which invention belongs] Especially this invention relates to a manufacture method of an MOS mold high-tension power element about semiconductor technology.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] the advantage which the impurity external diffusion which generate in a drift region minimize , it be [advantage] effective in improve the ON-resistance of a power element since it can prevent that the formation field of field oxide be expand , and do not decrease most breakdown voltage of a power element be by use the TEOS oxide film in which a low-temperature process be possible at the time of field oxide formation in the manufacturing process of an MOS mold high tension power element according to this invention , as having mentioned above .

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the above is in process, and in order to form field oxide 6, the thermal oxidation process of the long duration which advances at a 1000-degree C elevated temperature is needed. To that external diffusion of the impurity poured into the drift region 4 while the field oxide 6 formation process advanced in connection with this occurs, and coincidence Oxide-film growth to the side and the perpendicular direction by the BAZU beak (bird'sbeak) effect of field oxide in a lateral portion occurs. Since it is expanded from a layout value as the length of the formation field of field oxide 6 is shown by A from the length (layout value) of the mask pattern for forming field oxide 6, the trouble which ON-resistance comes to increase is induced.
[0009] This invention was made in order to cancel the trouble concerning the conventional example mentioned above, and it tends to offer the manufacture method of a high-tension power element that impurity external diffusion of a drift region is minimized, the length of a drift region is reduced, and ON-resistance can be improved.

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MEANS

[Means for Solving the Problem] The 1st step where a manufacture method of a high-tension power element concerning this invention forms the 1st well of the 1st conductivity type in an epitaxial layer of the semiconductor substrate upper part, The 2nd step which forms a drift region of the 2nd conductivity type, and the 2nd well of the 1st conductivity type in the 1st well of the above, The 3rd step which forms a TEOS oxide film in the whole structure upper part after the 2nd step execution of an account, The 4th step which forms field oxide which carries ut the selection chemical engraving of the above-mentioned TEOS oxide film, and defines an active region, the 5th step which forms the above-mentioned gate insulator layer and a gate electrode, and the 6th step which forms the source / drain field of the 2nd conductivity type in the above-mentioned active region are included.
[0011] Moreover, it is characterized by including further the 7th step which forms a pad oxide film of 200 thru/or 500A thickness in the whole structure upper part after the 2nd-step above-mentioned execution.
[0012] Moreover, it is characterized by the 3rd above-mentioned step coming to contain the 8th step which vapor-deposits the 1st TEOS oxide film of 5000 thru/or 8000A thickness on the above-mentioned pad oxide film, the 9th step which heat-treats the above-mentioned 1st TEOS xide film, and the 10th step which forms the 2nd TEOS oxide film of 2000 thru/or 3000A thickness on the above-mentioned 1st TEOS oxide film.
[0013] Moreover, the above-mentioned selection chemical engraving in the 4th above-mentioned step is characterized by using the dip etching method which used diluted HF solution.
[0014] Furthermore, it is characterized by for the 1st conductivity type of the above being N type, and the 2nd conductivity type of the above being P type.
[0015]
[Embodiment of the Invention] The 1st step where the high-tension power element manufacture method concerning this invention forms the 1st well of the 1st conductivity type in the epitaxial layer of the semiconductor substrate upper part, The 2nd step which forms the drift region of the 2nd conductivity type, and the 2nd well of the 1st conductivity type in the 1st well of the above, The 3rd step which forms a TEOS oxide film in the whole structure upper part after the 2nd-step above-mentioned execution, The 4th step which forms the field oxide 26 which carries out the selection chemical engraving of the above-mentioned TEOS oxide film, and defines an active region, the 5th step which forms the above-mentioned gate insulator layer and a gate electrode, and the 6th step which forms the source / drain field of the 2nd conductivity type in the above-mentioned active region are included.
[0016] Moreover, when forming field oxide in the manufacturing process of a high-tension power element, this invention vapor-deposits a TEOS oxide film instead of forming field oxide on a drift region using the existing LOCOS technology, carries out patterning of this, and forms field oxide. Therefore, ON-resistance is improved by not carrying out external diffusi n of the impurity of a drift region by shortening the length of a drift region and forming field oxide at low temperature.
[0017] The gestalt of desirable operation of this invention is explained that th se who had hereafter the information usual by th technical field to which this invention belongs can carry out this invention more easily. [0018] Drawing 1 thru/ r drawing 7 are having illustrated the

high-tension power element manufacturing process of P-channel concerning the gestalt of 1 operation of this invention, and explains the manufacturing process with reference to this hereafter.

[0019] First, the substrate with which the embedded oxide layer 21 and the P-epitaxial layer 22 were formed on the N-type s miconductor substrate 20 is used as illustrated t drawing 1 .

[0020] Subsequently, after pouring the Lynn (Phosphorus) ion into P-epitaxial layer as illustrated to drawing 2 , carry out heat treatment at 1200 degrees C for 25 hours, and the deep N-well 23 is formed. After forming the ion-implantation mask (not shown) which defines a drift field on the deep N-well 23, the ion implantation of the boron (B) is carried out as a P type impurity. After removing an ion-implantation mask, the ion-implantation mask (not shown) which defines N-well is formed on the deep N-well 23. After pouring in Lynn (P) as an N type impurity, the N-well 25 which carries out heat treatment between 15 hours at 1200 degrees C, and touches the P type drift region 24 and it is formed.

[0021] Next, after growing up the oxide film (not shown) of 200-500A thickness all over a substrate and making the TEOS oxide film of 5000-8000A thickness vapor-deposit by the 1st order as illustrated to drawing 3 , heat treatment is carried out at 850 degrees C. The field oxide 26 to which the field which etched the TEOS oxide film using **** (HF) diluted after vapor-depositing the TEOS oxide film of 2000-3000A thickness by the 2nd order, and was planned in the active region (the source / drain field, and gate field) of a power element is exposed is formed. A dip chemical engraving process is gone on and it is made for the side attachment wall f field oxide 26 to incline for formation of field oxide 26 at this time.

[0022] Subsequently, after oxidizing the whole surface of a substrate, growing up an oxide film and forming a polycrystalline silicon film in the upper part as illustrated to drawing 4 , the selection chemical engraving of a polycrystalline silicon film and the oxide film is carried out at rder using the mask for gate electrode formation, and gate oxide 27 and the gate electrode 28 are formed.

[0023]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is explanatory drawing of the manufacturing process of P-channel high-tension power element concerning the gestalt of 1 operation of this invention.
[Drawing 2] It is explanatory drawing of the manufacturing process following drawing 1.
[Drawing 3] It is explanatory drawing of the manufacturing process following drawing 2.
[Drawing 4] It is explanatory drawing of the manufacturing process following drawing 3.
[Drawing 5] It is explanatory drawing of the manufacturing process following drawing 4.
[Drawing 6] It is explanatory drawing of the manufacturing process following drawing 5.
[Drawing 7] It is explanatory drawing of the manufacturing process following drawing 6.
[Drawing 8] It is impurity distribution property drawing of each power element which used the TEOS oxide film by the conventional power element and conventional this invention using LOCOS technology.
[Drawing 9] It is current-voltage characteristic drawing of each power element which used the TEOS oxide film by the conventional power element and conventional this invention using LOCOS technology.
[Drawing 10] It is the cross section of P-channel high-tension power element formed by the conventional technology.
[Description of Notations]
20 A substrate, 21 An embedded oxide layer, 22 P-epitaxial layer, 23 Deep N-well, 24 A P type drift region, 25 N-well, 26 Field oxide, 27 Gate oxide, 28 A polycrystalline silicon film, 29 A drain field, 30 A source field, 31 An interlayer insulation film, 32 A metal electrode, 33 N+ mold source contact.

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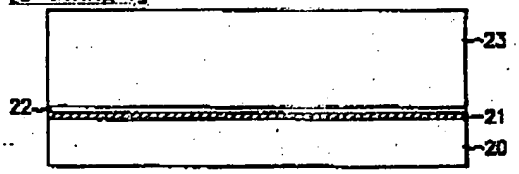
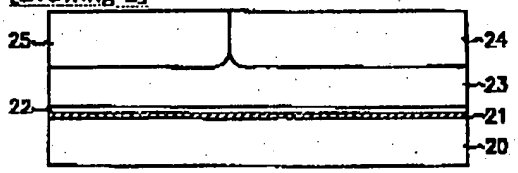
DRAWINGS

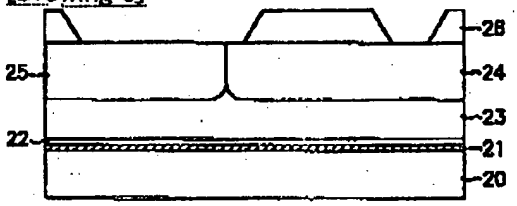
[Drawing 1]



[Drawing 2]



[Drawing 3]



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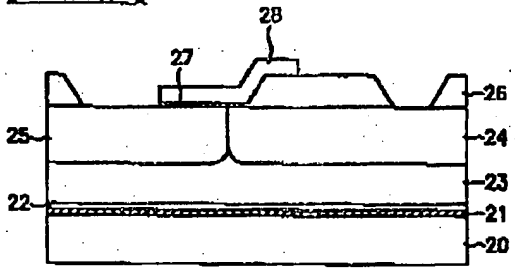
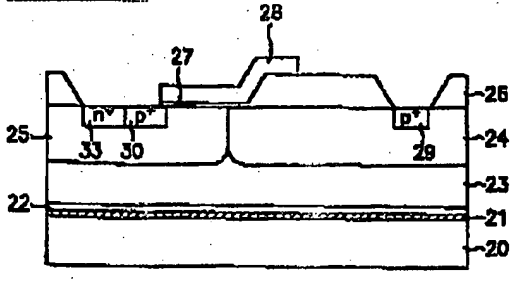


[Drawing 5]



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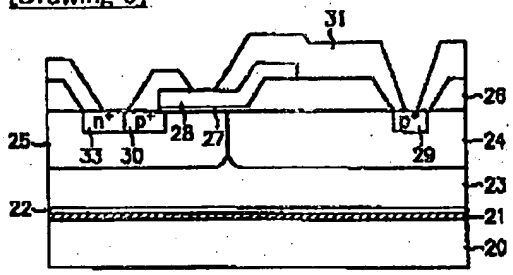
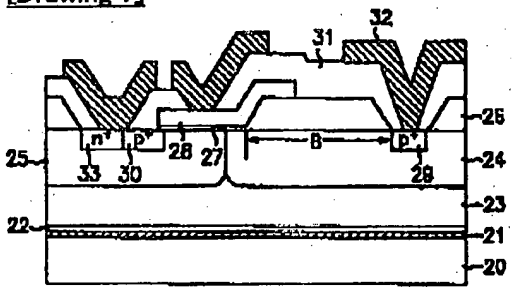
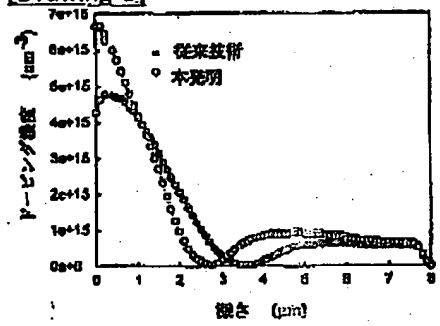


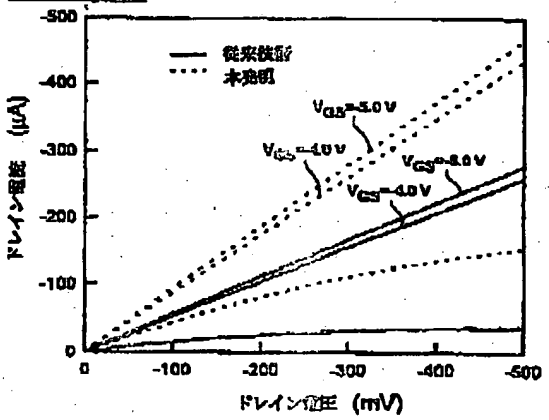
[Drawing 7]



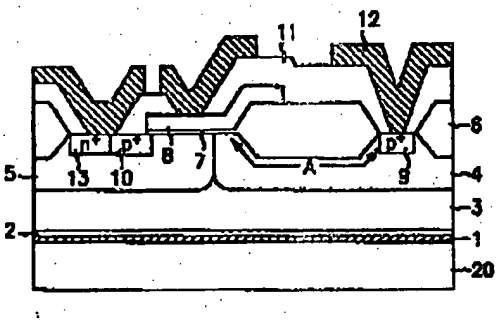
[Drawing 8]



[Drawing 9]



[Drawing 10]



[Translation done.]

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